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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/798,795	KILBUCK ET AL.	
	Examiner	Art Unit	
	HETUL PATEL	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,13-33,36-51,54-66,69-85 and 88-99* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,13-33,36-51,54-66,69-85 and 88-99* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the response filed on January 26, 2009. Claims 11-12, 34-35, 52-53, 67-68 and 86-87 were previously cancelled; and none of the claims are amended, cancelled or newly added in the current amendment. Therefore, claims 1-10, 13-33, 36-51, 54-66, 69-85 and 88-99 are currently pending in this application.

2. Applicant's arguments filed on January 26, 2009 have been considered but they are not deemed to be persuasive.

3. The rejection of claims 1-10, 13-33, 36-51, 54-66, 69-85 and 88-99 as in the previous Office Action is respectfully maintained.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 6-7, 10, 13, 17-31, 39-49, 54-62, 65, 70-76, 78-81, 84 and 89-99 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stobbs et al. (USPN: 2004/0039871) hereinafter, Stobbs in view of Lai et al. (USPN: 2003/0154370) hereinafter, Lai.

As per claim 1, Stobbs teaches a non-volatile memory device (i.e. 10 in Fig. 1) comprising:

- a non-volatile memory array (i.e. 24 in Fig. 1);
- a buffer memory (i.e. 182 in Fig. 3);
- a external synchronous memory interface (i.e. 58 in Fig. 2); and
- a controller (i.e. 172 in Fig. 3) coupled to the non-volatile memory array, the buffer memory, and the synchronous memory interface, wherein the controller is adapted to interface to and manage the non-volatile memory array and buffer memory and to present the non-volatile memory device as a synchronous memory device through the external synchronous memory interface (e.g. see Figs. 2-3 and paragraph [0033]).

However, Stobbs does not teach that the external synchronous interface is one of a SDRAM interface, a DDR interface, a DDR2 interface, GDDR interface, GDDR2 interface, and RDRAM interface; and the non-volatile memory device is adapted to present through the synchronous interface as one of a compatible read/write capable SDRAM device, a DDR device, a DDR2 device, a GDDR device, a GDDR2 device, and a RDRAM device. Lai, on the other hand, teaches that the synchronous interface is a SDRAM (i.e. SyncFlash DRAM) interface memory bus (see paragraph 3, lines 11-19), and the non-volatile memory device is adapted to present through the synchronous interface as SDRAM or DDR-SDRAM (i.e. SyncFlash DRAM). Accordingly, it would have been obvious to one of ordinary skills in the art at time of the current invention was made to use SDRAM and the SDRAM interface taught by Lai in the memory device taught by Stobbs. In doing so, it improves the speed/performance of the non-volatile memory device.

As per claims 2-3 and 6, the combination of Stobbs and Lai teaches the claimed invention as described above and furthermore, Stobbs teaches about buffering read and write data accesses to the non-volatile memory array in the buffer memory (e.g. see paragraph [0048]).

As per claims 4 and 7, the combination of Stobbs and Lai teaches the claimed invention as described above, but both of them failed to teach about buffering read data accesses in a least recently used manner and write data accesses in a write-through manner. However, it is well known and notorious old in the art that by buffering read data accesses in a least recently used manner and write data accesses in a write-through manner reduces the data latency and improves the overall performance of the memory device. The common knowledge or well-known in the art statement is taken to be admitted prior art because applicant failed to traverse the examiner's assertion of official notice made in the previous Office Action (see MPEP 2144.03 (C)).

As per claim 10, the combination of Stobbs and Lai teaches the claimed invention as described above and furthermore, Stobbs teaches that the non-volatile memory array (i.e. 102 in Fig. 3) of the non-volatile memory device (i.e. 100 in Fig. 3) is a Magnetoresistive Random Access Memory array (MRAM), Molecular Memory array, and Carbon Nanotube Memory array (e.g. see paragraph [0033] and Fig. 3).

As per claim 13, the combination of Stobbs and Lai teaches the claimed invention as described above and furthermore, Lai teaches that the non-volatile memory device is adapted to act as a BIOS boot memory device (see paragraph [0003], lines 15-19).

As per claim 17, the combination of Stobbs and Lai teaches the claimed invention as described above and furthermore, Lai teaches that the SDRAM (i.e. the SyncFlash DRAM, 14 in Fig. 1) is coupled to the controller (i.e. the DRAM memory controller) (see paragraph [0003], lines 10-15).

As per claims 18 and 19, the combination of Stobbs and Lai teaches the claimed invention as described above and furthermore, Lai teaches that the controller is adapted to selectively couple the DRAM memory array (using the chip select pins) to the synchronous memory interface; and selectively copy data from the non-volatile memory array and remap addresses of one or more DRAM memory array section to the synchronous memory interface to operate as "shadow" memory (e.g. see paragraphs [0031]-[0032] and [0035] and Figs. 2-3).

As per claims 20 and 21, the combination of Stobbs and Lai teaches the claimed invention as described above and furthermore, Lai teaches that the controller is adapted to operate the DRAM memory array (i.e. 14 in Fig. 1 and 22-23 in Fig. 2) as (i) an extended read and/or write data buffer memory (see paragraph [0004]); and (ii) as "scratch pad" memory, i.e. for storing boot code or any other data (e.g. see paragraph [0004]).

As per claims 22, 27, 44-45, 60, 75, 79, 94, 96 and 98-99, see arguments with respect to the rejection of claim 1. Claims 22, 27, 44-45, 60, 75, 79, 94, 96 and 98-99 are also rejected based on the same rationale as the rejection of claim 1.

As per claims 23, 29 and 47, see arguments with respect to the rejection of claim 2. Claims 23, 29 and 47 are also rejected based on the same rationale as the rejection of claim 2.

As per claims 24, 30, 48, 62, 76 and 81, see arguments with respect to the rejection of claim 3. Claims 24, 30, 48, 62, 76 and 81 are also rejected based on the same rationale as the rejection of claim 3.

As per claim 25, see arguments with respect to the rejection of claim 4. Claim 25 is also rejected based on the same rationale as the rejection of claim 4.

As per claims 26, 31, 49, 65, 78 and 84, see arguments with respect to the rejection of claim 6. Claims 26, 31, 49, 65, 78 and 84 are also rejected based on the same rationale as the rejection of claim 6.

As per claims 28, 46, 61, 80, 95 and 97, see arguments with respect to the rejection of claim 10. Claims 28, 46, 61, 80, 95 and 97 are also rejected based on the same rationale as the rejection of claim 10.

As per claim 54, see arguments with respect to the rejection of claim 13. Claim 54 is also rejected based on the same rationale as the rejection of claim 13.

As per claims 39-43, see arguments with respect to the rejection of claims 17-21. Claims 39-43 are also rejected based on the same rationale as the rejection of claims 17-21, respectively.

As per claims 55-59, see arguments with respect to the rejection of claims 17-21. Claims 55-59 are also rejected based on the same rationale as the rejection of claims 17-21, respectively.

As per claims 70-74, see arguments with respect to the rejection of claims 17-21. Claims 70-74 are also rejected based on the same rationale as the rejection of claims 17-21, respectively.

As per claims 89-93, see arguments with respect to the rejection of claims 17-21. Claims 89-93 are also rejected based on the same rationale as the rejection of claims 17-21, respectively.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stobbs in view of Lai, further in view of Widdup (USPN: 6,651,148).

As per claim 5, the combination Stobbs and Lai teaches the claimed invention as described above. However, none of them teaches that the controller is adapted to buffer a current data block to the non-volatile memory array in the buffer memory while accessing a sequentially following data block from the non-volatile memory array. Widdup, on the other hand, teaches about buffering both the read and write data (blocks) in the (buffer) memory to achieve the maximum bandwidth of the high-speed controller (e.g. see Col. 4, line 65 –Col. 5, line 1). Accordingly, it would have been obvious to one of ordinary skilled in the art at the time of the current invention was made to implement the teachings of Widdup in the memory device taught by the combination Stobbs and Lai so the maximum bandwidth of the high-speed controller can be achieved.

6. Claims 8, 32, 50, 63-64, 77 and 82-83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stobbs in view of Lai, further in view of Wallace et al. (USPN: 6,628,537) hereinafter, Wallace.

As per claim 8, the combination Stobbs and Lai teaches the claimed invention as described above. However, none of them teaches that the non-volatile memory device is adapted to indicate when the non-volatile memory device is busy by changing the status of one of an external "ready/busy" pin and a status register. Wallace, on the other hand, teaches that when the memory system is in process of executing a command and cannot receive another, a BUSY signal is written in the status register (i.e. 223 in Fig. 16) so the host computer wait until the current command/instruction is finish executing before sending the next one. Accordingly, it would have been obvious to one of ordinary skilled in the art at the time of the current invention was made to implement the teachings of Wallace in the memory device taught by the combination Stobbs and Lai so the possible data corruption is avoided.

As per claims 32, 50, 63-64, 77 and 82-83, see arguments with respect to the rejection of claim 8. Claims 32, 50, 63-64, 77 and 82-83 are also rejected based on the same rationale as the rejection of claim 8.

7. Claims 9, 33, 51, 66 and 85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stobbs in view of Lai, further in view of Meyer (USPN: 4,065,862).

As per claim 9, the combination Stobbs and Lai teaches the claimed invention as described above. However, none of them teaches that the non-volatile memory device

is adapted to indicate when the buffer memory device is full by asserting one of an external "ready/busy" pin and a status register. Meyer, on the other hand, teaches about asserting BUFFER FULL signal from the status register (i.e. 56 in Fig. 2), which would stop additional data to be sent to the buffer. Accordingly, it would have been obvious to one of ordinary skilled in the art at the time of the current invention was made to implement the teachings of Wallace in the memory device taught by the combination Stobbs and Lai so the possible data corruption is avoided by pausing the additional data transfer to the buffer memory while the buffer memory is full.

As per claims 33, 51, 66 and 85, see arguments with respect to the rejection of claim 9. Claims 33, 51, 66 and 85 are also rejected based on the same rationale as the rejection of claim 9.

8. Claims 14 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stobbs in view of Lai, further in view of Bartoli et al. (USPN: 6,442,068) hereinafter, Bartoli.

As per claim 14, the combination of Stobbs and Lai teaches the claimed invention as described above, but failed to teach that the non-volatile memory is adapted to have a burst data access mode. However, Bartoli teaches that the non-volatile memory is adapted to have a burst data access mode (e.g. see Col. 2, lines 11-15). Accordingly, it would have been obvious to one of ordinary skilled in the art at the time of the current invention was made to utilize the burst data access mode in the non-volatile memory as taught Bartoli in the memory device taught by the combination of

Stobbs and Lai. In doing so, (i) more data can be retrieved on each access; and (ii) it saves the bandwidth on the memory bus by sending less number of requests to the memory. Therefore, it is being advantageous.

As per claim 36, see arguments with respect to the rejection of claim 14. Claim 36 is also rejected based on the same rationale as the rejection of claim 14.

9. Claims 15-16, 37-38, 69 and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stobbs in view of Lai, further in view of the 'Background of the Invention' section of the current application, hereinafter, BOI.

As per claims 15 and 16, the combination of Stobbs and Lai teaches the claimed invention as described above, but failed to teach that the controller is adapted to generate and evaluate ECC data. BOI, however, teaches that the controller of the flash memory generates the ECC code so the errors of the flash memory can be addressed by the OS/host/driver/firmware and/or the file system that the flash memory system formatted with (e.g. see paragraph [0005]). Accordingly, it would have been obvious to one of ordinary skilled in the art at the time of the current invention was made to generate and evaluate the ECC data by the controller as taught by BOI in the memory device taught by the combination of Stobbs and Lai for the benefit(s) stated above. The further limitation of generating the ECC code in a hardware circuit is inherently present in the BOI because there has to be a hardware circuit present in order to generate the EC code.

As per claims 37, 69 and 88, see arguments with respect to the rejection of claim 15. Claims 37, 69 and 88 are also rejected based on the same rationale as the rejection of claim 15.

As per claim 38, see arguments with respect to the rejection of claim 16. Claim 38 is also rejected based on the same rationale as the rejection of claim 16.

Remarks

10. As to the remark, Applicant asserted that Stobbs et al. cannot be modified to use the SYNCFLASH memory or its interface as asserted by the Office Action as Stobbs et al. expressly teaches away from such combination in that its stated purpose is to replace Flash memory.

Examiner respectfully traverses Applicant's remark for the following reasons:

Examiner would like to point out to Applicant that Stobbs shows a prior art computer system (i.e. 10 in Fig. 1) having a flash RAM memory (i.e. 24 in Fig. 1). The flash RAM 24 has to have a controller and a temp ram inherently present in it similar to as shown and described in Fig. 3 for the magnetic memory 102. Fig. 3 and its description is referenced in the office action to show the inherent components (i.e. controller and temp buffer memory) of the flash RAM memory 24 similar to the replacement memory device 100 of Figs. 2-3. Since the Fig. 1 of the Stobbs reference does use the flash RAM memory, it is obvious and proper, in view of Lai, to modify it by

using SyncFlash DRAM and SDRAM interface bus as taught by Lai. Hence, the previous 103 rejection is proper and maintained.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Charlier et al. (USPN: 2002/0114211), "Asynchronous flash-EEPROM behaving like a synchronous RAM/ROM"

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HETUL PATEL whose telephone number is (571)272-4184. The examiner can normally be reached on 8:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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